TCET

DEPARTMENT OF ELECTRONICS ENGINEERING (ETRX)

Credit Based Grading Scheme(Revised - 2012) - University of Mumbai

CBGS-2012(R)

Estd. 2001

Semester Plan

TCET/FRM/IP-02/09 **(Theory)** **Revision: A**

Semester: VII **Course: ETRX**

Subject: EXC- 702:I C Technology **Class: BE ETRX**

S.No.	Prerequisite/ Bridge course:	Duration (Week /Hrs)	Modes of Learning	Recommended Sources
1	EXC302: Electronic Devices EXC303: Digital Circuits and Design EXC402: Discrete Electronic Circuits EXC502: Design With Linear Integrated Circuits EXC601: VLSI Design	6 hours	Self Learning/ Revision	**Textbooks:** 1.James D. Plummer, Michael D. Deal and Peter B. Griffin, "Silicon VLSI Technology" 2.Sorab K. Gandhi, "VLSI Fabrication Principles", Wiley, Student Edition. 3.Digital System 3.Principles & Design ... D.Roy Choudhary 4.Introduction To Logic Design. Alan B.Macrovin.

Class Room Teaching

Sr. No	Module No.	Lesson No	Topics Planned (Technology to be used)	Teaching Aids Required	Planned /Completion Date	Resource Book Reference	Remarks
1	Module 1	L1.1	SOP-Theory,Introduction to IC technology,Environment: Semiconductor technology trend, Clean rooms,	Power point presentation, Chalk & Board	07-11-2017	1.9:14-18	
2	Module 1	L1.2	SOP-OBE: Types : Semiconductor technology trend, Clean rooms, Wafer cleaning	Black Board & Chalk, Power point presentation	07-12-2017	All	
3	Module 1	L2.1	Semiconductor Substrate: Phase diagram and solid solubility.	Black Board & Chalk, Power point presentation	17/07/17	1.9:18-21	
4	Module 1	L2.2	Semiconductor Substrate: Crystal structure, Crystal defects, Czochralski growth.	Chalk & Board, Animation	18/7/2017	1.9:21-24	
5	Module 1	L2.3	Semiconductor Substrate: Bridgman growth of GaAs, Float Zone growth, Wafer Preparation and specifications	Chalk & Board, Animation	18/07/2017	1.9:26-29	
6	Module 1	L2.4	Semiconductor Substrate: Bridgman growth of GaAs, Float Zone growth	Black Board & Chalk, Power point presentation	19/07/2017	1.9:29-32	
7	Module 1	L3.1	Wafer Preparation and specifications	Black Board & Chalk, Power point presentation	24/7/2017	1.9:29-32	
8	Module 2	L3.2	Deposition: Evaporation, Sputtering and Chemical Vapor Deposition	Black Board & Chalk, Power point presentation	26/07/17	2.9:99-101	
9	Module 2	L3.3	Epitaxy: Molecular Beam Epitaxy, Vapor Phase Epitaxy	Black Board & Chalk, Power point presentation	26/07/17	2.3:99-101	
10	Module 2	L3.4	Epitaxy: Liquid Phase Epitaxy, Evaluation of epitaxial layers	Black Board & Chalk, Power point presentation	27/7/2017	2.9:100-101	
11	Module 2	L4.1	Silicon Oxidation: Thermal oxidation process, Kinetics of growth string	Chalk & Board, Animation	31/7/2017	2.9:78-81	

12	Module 2	L4.2	Silicon Oxidation: Properties of Silicon Dioxide, Oxide Quality, high κ and low κ dielectrics	Black Board & Chalk, Power point presentation	08-02-2017	2.9:78-81	
13	Module 2	L4.3	Diffusion: Nature of diffusion, Diffusion in a concentration gradient	Power point presentation, Chalk & Board	08-02-2017	2.9:39-41	
14	Module 2	L4.4	Diffusion: diffusion equation, impurity behavior, diffusion systems	Chalk & Board, Animation	08-03-2017	2.9:68-73	
15	Module 2	L5.1	Diffusion: problems in diffusion, evaluation of diffused layers	Chalk & Board, Animation	08-07-2017	2.9:68-73	
16	Module 2	L5.2	Ion Implantation: Penetration range, ion implantation systems, process	Black Board & Chalk, Power point presentation	08-09-2017	2.9:68-73	
17	Module 3	L5.3	Etching: Wet chemical etching, dry physical etching, dry chemical etching, reactive	Chalk & Board, Animation	08-09-2017	3.9:74-77	
18	Module 3	L5.4	Lithography: Photoreactive materials, Pattern generation and mask making	Black Board & Chalk, Power point presentation	08-10-2017	3.9:81-102	
19	Module 3	L6.1	Lithography: pattern transfer, Electron beam, Ion beam and X-ray lithography Application of Queues	Black Board & Chalk, Power point presentation	14/8/2017	3.9:81-102	
20	Module 3	L6.2	Device Isolation, Contacts and Metallization: Junction and oxide isolation, LOCOS	Black Board & Chalk, Power point presentation	16/8/2017	3.9:99-102	
21	Module 3	L6.3	Device Isolation, Contacts and Metallization: trench isolation, Schottky contacts, Ohmic contacts,	Black Board & Chalk, Power point presentation	16/8/2017	3.9:99-102	
22	Module 3	L7.1	CMOS Process Flow: N well, P-well and Twin tub	Chalk & Board, Animation	24/8/2017	3.9:86-100	
23	Module 3	L8.1	Design rules	Black Board & Chalk	30/8/2017	3.9:86-100	
24	Module 3	L8.2	Layout of MOS based circuits (gates and combinational logic), Buried and Butting Contact	Black Board & Chalk,	30/8/2017	3.9:86-100	
25	Module 4	L8.3	Semiconductor Measurements: Conductivity type, Resistivity, Hall Effect Measurements, Carrier	Black Board & Chalk, Power point presentation	31/8/2017	4.9:103-120	
26	Module 4	L8.4	Semiconductor Measurements: Drift Mobility, Minority Carrier Lifetime and diffusion length	Black Board & Chalk, Power point presentation	09-04-2017	4.9:103-120	
27	Module 4	L9.1	Packaging: Integrated circuit packages, Electronics package reliability	Black Board & Chalk, Power point presentation	09-06-2017	4.9:120-123	
28	Module 4	L9.2	Packaging: Integrated circuit packages, Electronics package reliability	Black Board & Chalk, Power point presentation	09-06-2017	4.9:120-123	
29	Module 4	L9.3	Testing: Technology trends affecting testing Sort	Chalk & Board, Animation	09-07-2017	4.9:123-124	
30	Module 4	L10.1	process and test equipment, test economics and product quality	Black Board & Chalk, Power point presentation	09-11-2017	4.9:123-124	
31	Module 5	L10.2	SOI Technology: SOI fabrication using SIMOX, Bonded SOI and Smart Cut	Black Board & Chalk, Power point presentation	13/9/2017	5.9:125-134	

32	Module 5	L10.3	SOI Technology: SOI fabrication using SIMOX, Bonded SOI & Smart Cut, PD	Chalk & Board, Animation	13/9/2017	5.9:125-134	
33	Module 5	L10.4	GaAs Technologies: MESFET Technology, Digital Technologies	Black Board & Chalk, Power point presentation	14/9/2017	5.9:134-139	
34	Module 5	L11.1	GaAs Technologies: MMIC technologies, MODFET and Optoelectronic Devices	Black Board & Chalk, Power point presentation	18/9/2017	5.9:134-139	
35	Module 5	L11.2	Silicon Bipolar Technologies: Second order effects in BJT Performance of BJT	Black Board & Chalk, Power point presentation	20/9/2017	5.9:139-145	
36	Module 5	L11.3	Silicon Bipolar Technologies: Performance of BJT, Bipolar processes and BiCMOS	Black Board & Chalk, Power point presentation	20/9/2017	5.9:139-145	
37	Module 5	L11.4	Multigate Device: Various multigate device configurations	Black Board & Chalk, Power point presentation	21/9/2017	6.9:146-150	
38	Module 6	L12.1	Device structure and important features	Black Board & Chalk, Power point presentation	25/9/2017	6.9:146-150	
39	Module 6	L13.1	Nanowire: Fabrication and applications	Black Board & Chalk, Power point presentation	10-02-2017	6.9:150-151	
40	Module 6	L13.2	Nanowire: Fabrication and applications	Power point presentation, Chalk & Board	10-04-2017	6.9:150-151	
41	Module 6	L13.3	Graphene Device: Carbon nanotube transistor fabrication Algorithm	Black Board & Chalk, Power point presentation	10-04-2017	6.9:151-153	
42	Module 6	L13.4	Graphene Device: CNT applications	Black Board & Chalk, Power point presentation	10-05-2017	6.9:151-153	
43	Module 1,2	L14.1	Revision and presentation	Chalk & Board, Animation	10-09-2017	154-157	
44	Module 3,4	L14.2	Revision and presentation	Black Board & Chalk, Power point presentation	10-12-2017	154-157	
45	Module5, 6	L1.3	Revision 1,2	Black Board & Chalk, Power point presentation	17/7/2017	154-157	
46	Module 6	L2.5	Revision 3,4	Black Board & Chalk, Power point presentation	29/7/2017	154-157	
47	Module 6	L3.5	Revision 5,6	Black Board & Chalk, Power point presentation	08-05-2017	154-157	
48	Module 6	L15.1	University paper solving	Black Board & Chalk, Power point presentation	16/10/2017	154-157	
49	Module 6	L15.2	University paper solving	Black Board & Chalk, Power point presentation	17/10/2017	154-157	
50	Module 6	L15.3	University paper solving	Black Board & Chalk, Power point presentation	17/10/2017	154-157	

Remark:			
Course:	Syllabus Coverage:	Practice Session: 2	**Content Beyond Syllabus:** CAD Tool,SOI tecnologies and multigate transistor technologies CAD Tool
No. of (lectures planned)/(lecture taken): 50/			

Advanced course: IC Technology	20 Hours	Online NPTEL videos	**Web sources:** 1. NPTEL-https://onlinecourses.nptel.ac.in 2. www.tutorialpoint.com1. Instructor's study material, **Textbook reference:** 1. G. S. May and S. M. Sze, "Fundamentals of Semiconductor Fabrication",

Text Books:

1. James D. Plummer, Michael D. Deal and Peter B. Griffin, "Silicon VLSI Technology", Pearson, Indian Edition.
2. Stephen A. Campbell, "The Science and Engineering of Microelectronic Fabrication", Oxford University Press, 2nd Edition.
3. Sorab K. Gandhi, "VLSI Fabrication Principles", Wiley, Student Edition.
4. G. S. May and S. M. Sze, "Fundamentals of Semiconductor Fabrication", Wiley, First Edition.

Reference Books:

1. Kerry Bernstein and N. J. Rohrer, "SOI Circuit Design Concepts", Kluwer Academic Publishers, 1st edition.
2. Jean-Pierre Colinge, "FinFETs and Other Multigate Transistors", Springer, 1st edition
3. M. S. Tyagi, "Introduction to Semiconductor Materials and Devices", John Wiley and Sons, 1st edition.
4. James E. Morris and Krzysztol Iniewski, "Nanoelectronic Device Applications Handbook", CRC Press
5. Glenn R. Blackwell, "The electronic packaging", CRC Press 10. Michael L. Bushnell and Vishwani D. Agrawal, "Essentials of Electronic Testing for digital, memory and mixed-signal VLSI circuits", Springer

Digital Reference:

3.1 https://www.mosis.com/
3.2 www.tutorialpoint.com

Name & Signature of Faculty Signature of HOD Signature of Principal /Dean (Academics)

Date: Date: Date:

Note:

1. Plan date and completion date should be in compliance
2. Courses are required to be taught with emphasis on resource book, course file, text books, reference books, digital references etc.
3. Planning is to be done for 15 weeks where 1st week will be AOP, 2nd -13th for effective teaching and 14th -15th week for effective university examination oriented teaching, mock practice session and semester consolidation.
4. According to university syllabus where lecture of 4 hrs/per week is mentioned minimum 55 hrs and in case of 3 lectures per week minimum 45 lectures are to be engaged are required to be engaged during the semester and therefore accordingly semester planning for delivery of theory lectures shall be planned.
5. In order to improve score in NBA, faculty members are also required to focus course teaching beyond university prescribed syllabus and measuring the outcomes w.r.t learning course and programme objectives.
6. Text books and reference books are available in syllabus. Here only additional references w.r.t. non –digital/ digital sources can be written (if applicable)
7. Technology to be used in class room during lecture shall be written below the topic planned within the bracket.